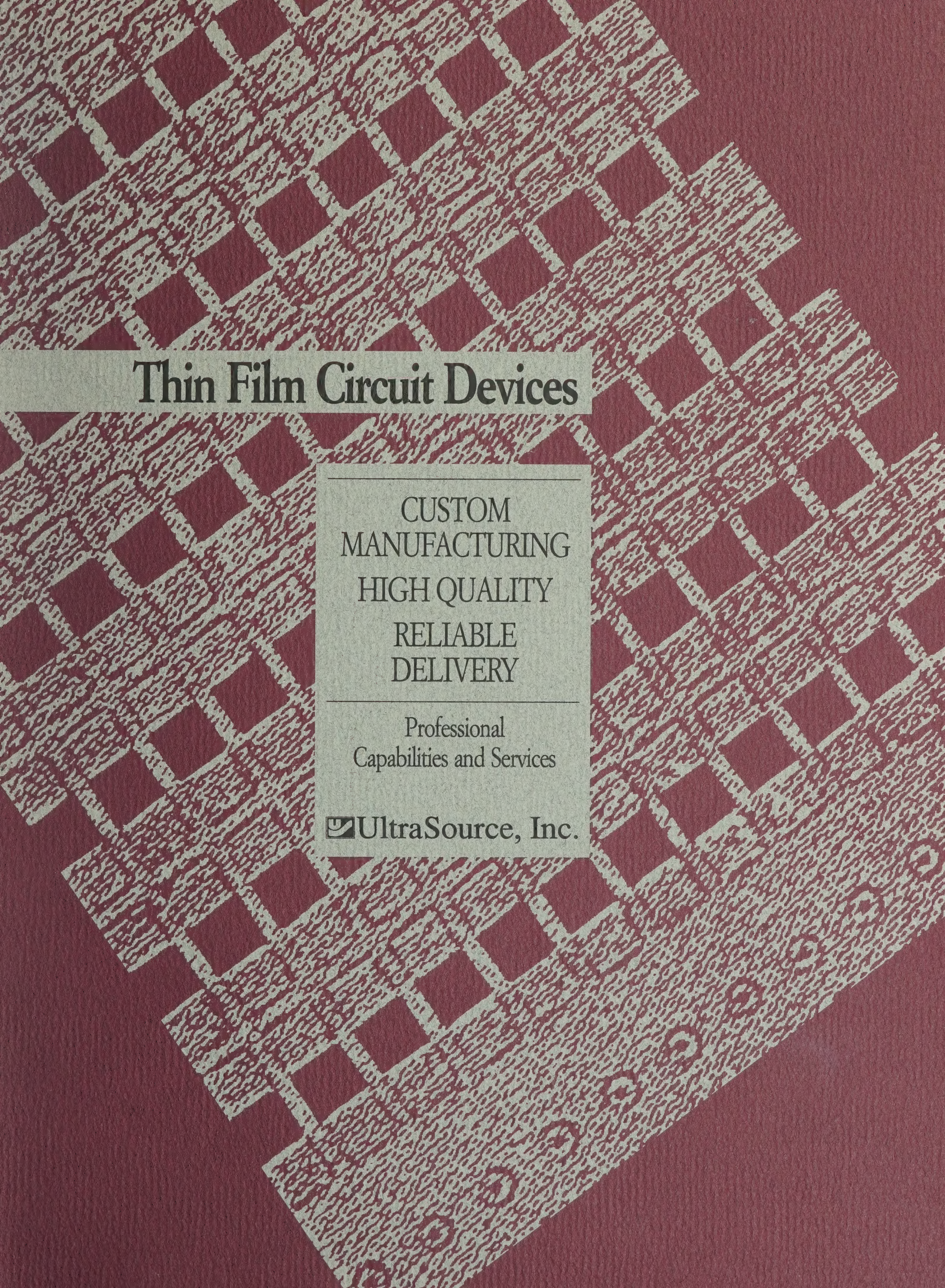

Thin Film Circuit Devices

CUSTOM
MANUFACTURING
HIGH QUALITY
RELIABLE
DELIVERY

Professional
Capabilities and Services

UltraSource, Inc.

Custom Manufacturing of Thin Film Circuit Devices

UltraSource, Inc. is a custom manufacturer of thin film circuit devices supplying our customers with the highest quality product, matchless technical sales support, and prompt, reliable delivery. We fabricate devices on many different substrate materials with filled thermal vias, conductors, sheet resistors, plated-through holes, slots, and edge wrap-arounds.

Broad Experience

Our customer list includes TRW, Allied Signal, ITT Avionics, Martin Marietta Laboratories, Texas Instruments, Raytheon Company, Alpha Industries, Philips Electronics Laboratories, Rockwell International, and many medium and small size specialized electronics firms.

The high reliability and quality of our thin film circuit devices allow them to be used in many demanding commercial and defense-related applications such as telecommunications, imaging and printing systems, radar and signal transmission, and medical equipment. Our circuits have been employed in cellular and wireless communications systems, DC to 64 GHz microwave devices, ink-jet printheads, pacemaker devices, and microwave calibration fixtures, among others.

Professional Capabilities and Services

Design Engineering: We provide comprehensive design guideline literature and custom design assistance on all aspects of thin film circuit device fabrication.

Substrate Materials: UltraSource, Inc. supplies circuit devices made of alumina, beryllium oxide, aluminum nitride, fused silica, ferrites, titanates, glass, and plastic materials. Many of these materials are stocked in as-fired and polished conditions, readily available for delivery. We currently offer polished alumina, beryllium oxide, and aluminum nitride substrates with planar thermal vias filled with pure copper.

Thin Film Coatings: We offer the highest quality sputtered, electroless, and electrolytic coatings available. Conductor, barrier, and resistor films are routinely applied to many different circuit and substrate designs.

Patterning and Etching: We maintain pattern-plate and etch-back processes which enable us to custom fabricate gold and copper conductors, plated-through holes, sheet resistors, nickel barrier layers, and edge wrap-arounds. Using your supplied design data, we develop and use phototooling to manufacture quality, cost effective circuit devices.

Substrate Machining: We use many methods such as CO_2 laser machining of substrates, YAG laser trimming of sheet resistors, CO_2 laser scribing, diamond sawing (dicing), and ultrasonic impact grinding to shape and form substrate materials.

Total Commitment to Quality: At UltraSource, Inc. we strive to ensure that our quality efforts provide the highest levels of product reliability and customer satisfaction. We believe that concise, accurate design assistance, exact conformance to your specifications, prompt customer service, and timely delivery is owed to every customer. This "Total Quality" pledge is our commitment to you.

Call us today.

We provide free, timely quotations and work from your supplied prints, sketches, CAD files, grid drawings, etc. to deliver devices to you when you need them. We stock a large variety of sputtered substrates, so prototypes can normally be delivered in 1-3 weeks. Custom metallizations, plated-through hole designs, thermal via products, and most production orders are supplied in 3-6 weeks, depending on complexity.

Call us toll free any time at (800) 742-9410 for more information.

UltraSource, Inc.

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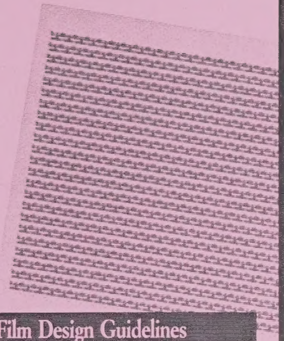


Thin Film Design Guidelines

Substrates

- Polished and as-fired 99.5% and 99.6% alumina, beryllium oxide, aluminum nitride, and fused silica substrates commonly in stock.

Material surface finishes (μinches CLA):

	As-Fired	Polished
99.5% Alumina	< 6	< 2
99.6% Alumina	< 4	< 2
Beryllium Oxide	< 5	< 3
Aluminum Nitride	< 32	< 3
Fused Silica	N/A	< .2

- Standard tolerances on substrate thickness: ± 10% for as-fired materials and ± .001" or ± .0005" for polished materials.

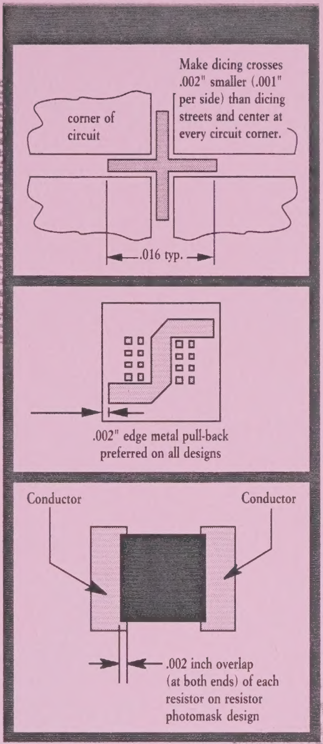
Filled Thermal Vias

- Alumina, beryllium oxide, and aluminum nitride substrates can be supplied with filled, planar vias of pure copper offering excellent thermal conductivity and low inductance at high operating frequencies.
- Our filled via process is available on polished substrates only and is compatible with all metal systems as long as the vias are surrounded by annular pads at least .004" larger in diameter than the vias.
- Available via diameters are:

substrate thickness	allowable diameters
.010"	.005 – .010"
.015"	.007 – .015"
.020"	.008 – .020"
.025"	.010 – .020"

Metallization

- *Conductors only:* recommended metallization is 500Å ± 5% of tungsten-titanium (WTi) under 100-220 μinches of gold (Au). Au thickness is dependent on assembly requirements and should be toleranced to ± 10%. Nickel (2000-5000Å) may also be added between the WTi and Au layers to add solderability to the circuit. NiCr/Au and NiCr/Ni/Au metallizations are also available.
- *Resistors and conductors:* recommended metallization is 50-200 ohms/square of tantalum-nitride (TaN) under 500Å ± 5% WTi under 100-220 μinches of gold (Au). Nickel (2000-5000Å) may also be added between the WTi and Au layers to add solderability to the circuit. Au thickness is dependent on assembly requirements and should be toleranced to ± 10%. Low TCR NiCr/Au and NiCr/Ni/Au films are also available.


Make dicing crosses .002" smaller (.001" per side) than dicing streets and center at every circuit corner.
corner of circuit
.016 typ.
.002" edge metal pull-back preferred on all designs
Conductor
Conductor
.002 inch overlap (at both ends) of each resistor on resistor photomask design

Etching and Patterning

- Preferred minimum line and space widths are .002" but line widths and spaces can be supplied as small as .0005" wide.
- Standard line and space width tolerancing is ± .001, ± .0005, or ± .0002"; however, tolerancing as tight as ± .0001" is available.
- Half via or diced slots are the preferred wrap-around design method.
- Annular rings or pads around plated-through geometries should be at least .005" wide.

Sheet Resistors

- Resistors can be supplied to ± 20% of the nominal values without laser trimming.
- Laser trimming can be used to trim resistors to standard values of ± 10%, 5%, 2%, 1%.
- Preferred laser trimming methods (ie: scrub cut, serpentine, plunge cut, etc.) should be specified on drawings or RFQ's.
- Standard minimum trim width guidelines are a 50% reduction in resistor width or .002", whichever is larger.

Laser Drilled Holes and Machined Features

- Minimum hole diameters for both plated and non-plated through geometries should be equal to ½ the substrate thickness.
- Standard tolerance on hole diameters: ± .002".
- Standard hole-to-hole location tolerances: ± .001", non-cumulative.
- Standard shape tolerance on machined geometries: ± .002".
- Minimum spacing between holes or machined geometries should not be less than a distance equal to the substrate thickness.

Dicing (Diamond Sawing)

- Standard dicing street width is .006" wide for substrates .005" to .025" in thickness and .010" wide for substrates .030" to .050" thick.
- The preferred tolerance on length and width of diced circuits is ± .003", but ± .002" or ± .001" tolerancing is available.
- In order to avoid gold "overhang" on the edges of diced circuits it is requested that dicing crosses be designed .002" (.001" per side) smaller than the actual dicing street width and inserted on CAD files at the corner of every circuit device.
- Conductor lines which extend to the edge of a circuit should be pulled back .002" on CAD files to keep the soft conductor metallization out of the path of the dicing saw.

Photomasks

- Mylar masks should be supplied 5" x 7" with the photo image in the center of the mask.
- Glass masks should be chrome (or iron-oxide if plated through holes are included in the design) and 4" x 4", with the photo image centered in the middle of the mask.
- Separate masks must be supplied for conductor and resistor layers.
- All *conductor* masks should be supplied negative image (ie: circuit clear with dark background) right reading with the emulsion down, no etch factors.
- All *resistor* masks should be supplied positive image (ie: circuit dark with clear background) right reading with the emulsion down, no etch factors.
- The length of each resistor image (on the resistor mask) should be increased by .002" on CAD files at each location where a resistor contacts a conductor.
- Photomasks can be generated from drawings, rubyliths, DXF format cad files, or AutoCAD drawing files.

Ordering Information

- Please use our Request For Quotation sheet when placing an order or sending an RFQ. It asks all of the pertinent questions we need answered to serve you properly and will save time and effort.
- We look forward to working with you! Please feel free to call us any time at **(800) 742-9410** or fax us at **(508) 251-8686**.

UltraSource, Inc.
166B Middlesex Street
N. Chelmsford, MA 01863

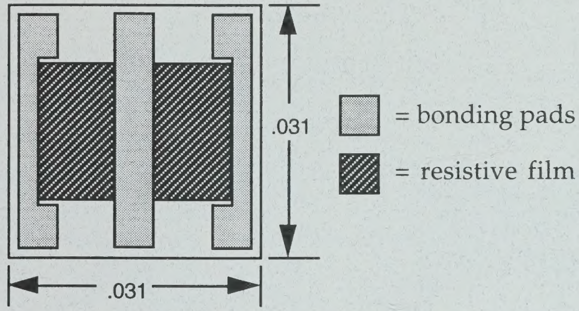
UltraSource, Inc.

166B Middlesex Street • N. Chelmsford, MA 01863 • (508) 251-4884 • Fax (508) 251-8686

THIN FILM SILICON CHIP RESISTORS

UltraSource, Inc. offers high quality custom manufactured precision silicon thin film chip resistors for the hybrid and microwave industries. Our Tantalum-Nitride (TaN) chip resistors are available on polished silicon material in many different sizes with resistances values of 1 ohm through 100Kohms. Stock and custom sizes are available.

• SAMPLE SPECIFICATION •



- Tantalum-Nitride (TaN) films exhibit excellent long term stability and moisture resistance in most environments.
- 11,000Å silicon dioxide insulating layer is standard
- Lapped backside surface is standard

• Bonding Pads •
Can be GOLD ONLY for wire bonding attachment

• ELECTRICAL SPECIFICATIONS •

• Resistance Values Tolerances •
± .1% thru ± 10%

• Long Term Resistance Stability •
<.1% drift over 1,000 hours at 125°C

• Operating Temperature Range •
-55°C to 150°C

• Power Handling Capability •
Approximately 50 Watts per square inch

• Temperature Coefficient of Resistance (TCR) •
TaN films = -100 ± 50 ppm/°C

- continued on other side -

UltraSource, Inc.

166B Middlesex Street • N. Chelmsford, MA 01863 • (508) 251-4884 • Fax (508) 251-8686

THIN FILM SILICON CHIP RESISTORS

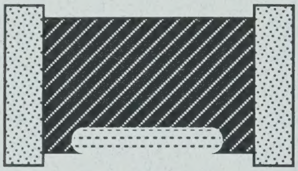
• GENERAL INFORMATION•

- Typical recommended chip thickness is .010 ± .002" silicon.

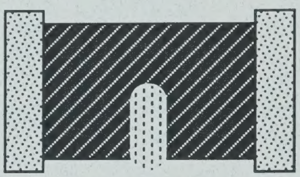
- Insulating layer is 11,000Å of thermally grown silicon dioxide.

- GOLD ONLY metalization is TaN under 500Å WTi under 50 μ-inches minimum of fully sputtered pure gold.

- Resistors are laser trimmed into tolerance using a "SCAN" cut laser trim (whenever possible) which is a trim style that works best for high frequency applications (see figure below).



scan trim



plunge trim

- If a design requires more trimming than scan cuts offer then a "PLUNGE" style trim method is used (as shown above).

- Normal laser trimming guidelines allow for up to a 50% reduction in original resistor width.

- TCR is calculated using the formula: $\text{TCR} \approx \dfrac{R_2 - R_1}{R_T(T_2 - T_1)}$

where the resistances are measured at temperatures $T_2 > T > T_1$ with T being room temperature.

- Standard resistor chip packaging is in Fluoroware chip tray carriers.

*** CALL US TOLL FREE AT (800) 742-9410 TO DISCUSS YOUR REQUIREMENTS ***

UltraSource, Inc.

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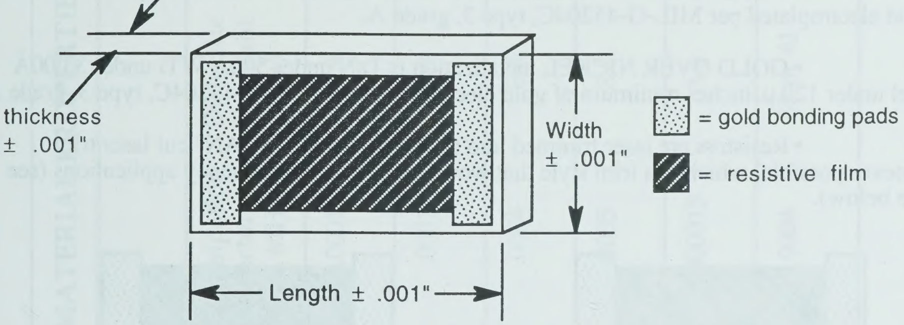
THIN FILM ALUMINA CHIP RESISTORS

UltraSource, Inc. offers high quality custom manufactured precision 99.6% alumina thin film chip resistors for the hybrid and microwave industries. Our Tantalum-Nitride (TaN) or Nichrome (NiCr) chip resistors are available on polished 99.6% alumina material in many different sizes with resistances values of 1 ohm through 100Kohms. Stock and custom sizes are available.

• SAMPLE SPECIFICATION •



Tantalum-Nitride (TaN) films exhibit excellent long term stability and moisture resistance in most environments.

Nichrome (NiCr) films exhibit low TCR and excellent long term stability when packaged in a protected environment.

• Bonding Pads •
Can be GOLD ONLY for wire bonding attachment
or
GOLD OVER NICKEL for wire bonding or tin-lead soldering attachment

• ELECTRICAL SPECIFICATIONS •

• Resistance Values Tolerances •
± .1% thru ± 10%

• Long Term Resistance Stability •
<.1% drift over 1,000 hours at 125°C

• Operating Temperature Range •
-55°C to 150°C

• Power Handling Capability •
Approximately 50 Watts per square inch

• Temperature Coefficient of Resistance (TCR) •
TaN films = -100 ± 50 ppm/°C
NiCr films = 0 ± 50 ppm/°C

- continued on other side -

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THIN FILM ALUMINA CHIP RESISTORS

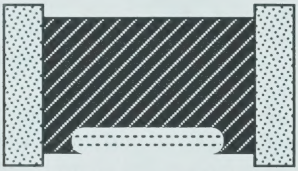
• GENERAL INFORMATION•

• Typical recommended chip thickness is .010 ± .001" except that .020" x .020" resistor chips are fabricated on .005 ± .0005" thick polished alumina.

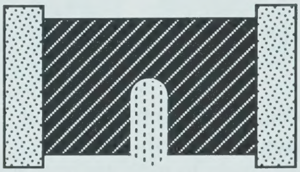
• GOLD ONLY metalization is TaN under 500Å WTi under 120 µ-inches minimum of gold electroplated per MIL-G-45204C, type 3, grade A.

• GOLD OVER NICKEL metalization is TaN under 500Å WTi under 3,000Å Nickel under 120 µ-inches minimum of gold electroplated per MIL-G-45204C, type 3, grade A.

• Resistors are laser trimmed into tolerance using a "SCAN" cut laser trim (whenever possible) which is a trim style that works best for high frequency applications (see figure below).



scan trim



plunge trim

• If a design requires more trimming than scan cuts offer then a "PLUNGE" style trim method is used (as shown above).

• Normal laser trimming guidelines allow for up to a 50% reduction in original resistor width.

• TCR is calculated using the formula: $\mathrm{TCR} \approx \dfrac{R_2 - R_1}{R_T(T_2 - T_1)}$

where the resistances are measured at temperatures $T_2 > T > T_1$ with T being room temperature.

• Standard resistor chip packaging is in Fluoroware chip tray carriers.

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SUBSTRATE MATERIAL PROPERTIES

Material	CLA Surface Roughness (μ-inches)	Thickness Tolerance	Dissipation Factor at 1 MHz	Dielectric Constant (k)	Thermal Conductivity (W/mK)	Thermal Expansion (μ-inches/°C)
As-fired 99.6% Alumina	<4	± 10% or ± 5%	.0001	9.9	30	7.1
Polished 99.6% Alumina	<2	±.001 or ± .0005	.0001	9.9	30	7.1
Polished 99.5% Beryllium-Oxide	<3	± .001 or ±.0005	.0004	6.5	250	9.0
Polished Aluminum Nitride	<3	± .001 or ±.0005	.0005	8.6	170	4.6
Polished Fused Silica	<.1	± .001 or ±.0005	.000015	3.8	1	.56
Polished Barium Titanate	<3	± .001 or ±.0005	.0004	38 or 41	1.8	5.8

Reprinted from "*Thin Film Circuit Design & Manufacturability Guidelines*"
presented by Michael D. Casper of UltraSource, Inc. at the
Wireless Technology Conference in September of 1995
• copies are available upon request •

UltraSource, Inc.

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UltraSource, Inc.
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Lockheed Martin
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M/A COM Inc.
Wienschel, Inc.
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MIT Lincoln Labs
Hittite Microwave Corporation
Siemens Pacesetter
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UltraSource, Inc.

166B Middlesex Street N. Chelmsford, MA 01863
Tel: (800)742-9410 Fax: (508)251-8686

• REQUEST FOR QUOTATION •

COMPANY: ____________ CONTACT(S): ____________
ADDRESS: ____________ ____________
____________ TELEPHONE: ____________
____________ FAX: ____________

PART NUMBER(S): ____________
APPLICATION: ____________
____

• PLEASE ATTACH BLUEPRINT OR SKETCH FOR CLARIFICATION •

CIRCUIT PARAMETERS:

- Circuit length ________ width ________ tolerance ________
- Substrate material ____________
- Substrate thickness ________ tolerance ________
- Surface finish on front side ________ backside ________

- Front metallization: layer #1 ________ thickness ________
  layer #2 ________ thickness ________
  layer #3 ________ thickness ________
  layer #4 ________ thickness ________

- Back metallization: layer #1 ________ thickness ________
  layer #2 ________ thickness ________
  layer #3 ________ thickness ________
  layer #4 ________ thickness ________

- Smallest line width or space ________ tolerance ________
- Through-holes (qty and dia.) ____________
- Plated-through holes (qty and dia.) ____________
- Filled-Via holes (qty and dia.) ____________
- Thin Film Resistors:
  value ranges (ohms) ________ tolerances (%) ________
  preferred trim style ________ min. trim width ________

PHOTOTOOLS:

- Photomask(s) exist ( ) yes ( )no
- UltraSource to manufacture photomask(s) from:
  ( ) Drawing ( ) CAD file ____________
  ( ) Other ____________

ORDERING INFORMATION:

- Circuit quantities to quote: ____________
- Requested delivery dates: ____________
- Anticipated production quantities/year ____________

Conversion-To-Gerber Requirements & Recommendations

Introduction

DXF is one of the most popular database exchange formats used today. There are several CAD packages that offer the designer/engineer many options to generate data for numerous applications.These applications, mostly mechanical, greatly satisfy the requirements needed in the industry. Unfortunately, the output for generating a precision artwork from these products has been limited to paper printers and penplotters. Although workable with most file conversions, we have found limitations in various output applications prompting us to write our own programs for data conversion. Of course, if you have a program that works for you, by all means continue to use it. By following certain design guidelines, Advance Reproductions can offer a viable method for data conversion.

Constraints

- Max number of layer names: 64 (This includes empty layers as well.)
- Max number of block definitions is: 128 (even if not inserted or used.)
- Max number of lines per layer, per block: 32000
- Max number of closed figures per layer, per block: 8000

Layering

Layering designation of your database is very important. Using numeric values for identifying layers works best when combining levels. It should be stated in your instructions as to which layers are to be utilized and which levels are to be combined.

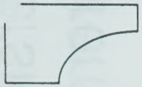
ULTRASOURCE

advance
reproductions corporation

Common Drawing Errors

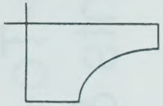
CAD Data

Open figures



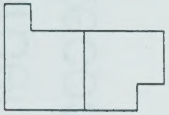
If lines and arcs are not continuous, and if they are not closed properly, data conversion will be difficult. This is an example of where a SNAP to grid modifier should be used.

Endpoints that do not meet



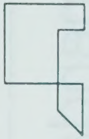
When endpoints do not meet the conversion process will not work. This example is overly exaggerated. However, in many instances the overlap is not as visible as the example illustrates.

Touching figures sharing a common line segment



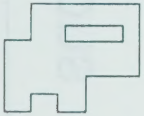
This problem arises when the line in the center is shared by two figures. The line can only be a part of one figure. A solution would be to digitize a zero width closed boundary to form each figure.

Figures that self intersect



The fill routine will not work correctly when a line intersects itself.

Figures within figures



The draftperson intended that the inner window should appear clear on the film. However, the outer polygon covered it . Put the inner polygon on a different layer or draw around it.

Hybrid Applications

Recommended Drawing Practices

- Advance will translate one layer at a time.
- Linetypes should be continuous. (In AutoCAD for example, the PEDIT, Join and Close commands are recommended.)
- Digitize utilizing good drafting procedures. (Snap to a grid.)
- Hatching is not necessary to fill figures; however, if hatch lines are present they will be translated to Gerber draw commands thus increasing conversion time. You must specify the hatch width sizes.
- Three dimensional coordinates and parameters are not used by Advance Reproductions.
- No layer or block should be named the same as the DXF file name.
- Keep the block and layer names unique and within 8 characters long. (Use numbers for layers.)
- Supply a one up image only with instructions to step and repeat if necessary.
- Make each single image into a block.

Defining Closed Figures

The best way to define a boundary of any shape is to digitize a line with a zero width by connecting end to end any combination of lines and arcs. (When using AutoCAD use the PLINE command.) Good drafting procedures should be followed. To insure acceptable data, the SNAP command should be turned on. Digitizing to a grid achieves a more precise database which will easily convert to Gerber. The line that forms the boundary should be continuous. In AutotCAD a command such as PEDIT will allow you to Join and Close a PLINE, thus creating a continuous line. No extra lines or arcs should be near or touching any of the vertices of your closed figure. Such commands as TRIM, FILLET, EXTEND, CHAMFER and BREAK can all be used to clean up your figures.

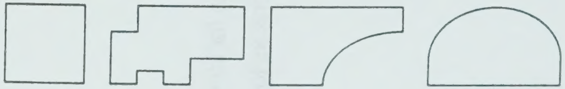


Fig 1. All of the figures shown above are drawn from lines and arcs. This example was drawn with AutoCAD 10 using a PLINE with a zero width. The last segment of each figure was made with the Close command.

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